

Shreyash Pandey

fp32.org | shreyash335@gmail.com | [LinkedIn](#) | [GitHub](#)

Systems Software Engineer with interest in Compilers, ML Compilers, LLMs and Open Source Software.

Experience

Systems Software Engineer

Vicharak

Aug 2023 – Aug 2025

- Architected an FPGA based edge-ML accelerator, and designed hardware building blocks (e.g., im2col, systolic arrays).
- Developed cycle-accurate simulators for architectural verification, performance profiling, and design tradeoff analysis.
- Designed and implemented a dataflow compiler, integrating graph-level (layer fusion, tiling) and ISA-specific hardware optimizations to achieve real-time (20-30fps) inference of image recognition and object detection workloads on low-power edge device.
- Developed a high-throughput runtime engine for edge deployment, including optimized NEON kernel development for ARM processors.
- Investigated hyper-quantized (Binary, Ternary) neural networks for their efficacy to be deployed on FPGAs

Linux Kernel Engineer (Intern)

Vicharak

Jan 2023 – Aug 2023

- Carried out research on potential applications of a heterogeneous FPGA based SBC
- Ported Tianocore EDK2 to Rockchip RK3588

Talks

- **No-ISA is the Best ISA** - Shreyash Pandey, Rishik Ram at IICT 2024, Bangalore [\[URL\]](#) [\[Summary\]](#)

Projects

- [Clogwave](#): An LLVM pass that instruments C code with VCD dumping callbacks that generate a VCD dump when input programs are run. When viewed in a tool like gtkwave, complex control flow can be easily visualized and mapped.
- [Open Source Contributions @ LLVM](#): Contributing to various areas of the llvm-project including libc, SelectionDAG, making intrinsics constexpr, and finding/fixing missed-optimizations. Primary project involves porting libc to MacOS/darwin and building clang with LLVM libc.
- fp32.org: A collection of long-form posts on technical topics ranging from FPGAs and reconfigurable computing to nitty-gritty of LLVMs codebase.
- [Atari 2600 Emulator](#): Engineered a functional Atari 2600 emulator in C and libSDL. Modeled the system's core components, including the 6502 CPU, Television Interface Adaptor (TIA), and RAM, I/O, and Timer (RIOT) chips. Developed a 6502 assembler and disassembler to support custom code and debugging.

Skills

C C++ Bash Python UV x86 Assembly ARM Assembly RISC-V Verilog PyTorch Onnxruntime
Tensorflow Tinygrad CUDA TensorRT LLVM ONNX Protobufs Markdown RST Sphinx Git
Make CMake GDB Valgrind Compiler Explorer Linux Windows ARM x86 6502
VLIW Architectures

Education

B.E in Computer Science Engineering

Aug 2019 – May 2023

G.H. Rasoni Institute of Engineering and Technology, Nagpur